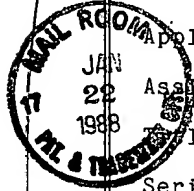


## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



Applicant: Richard A. Blanchard  
 Assignee: Siliconix Incorporated  
 Title: "PLANAR VERTICAL CHANNEL DMOS STRUCTURE"  
 Serial No.: 06/843,454 Filing Date: 3/24/86  
 Examiner: T. Thomas Art Unit: 114  
 Attorney Docket No.: M-300 US

Santa Clara, California  
 January 15, 1988

COMMISSIONER OF PATENTS & TRADEMARKS  
 Washington, D. C. 20231

SUPPLEMENTAL AMENDMENT

Sir:

Please add Claim 18 as follows:

18. The method of claim 17 wherein at the conclusion of said step of etching a plurality of grooves, each said grooves divide said second region into a plurality of semiconductor regions of said second conductivity type, and wherein said plurality of grooves laterally surround said plurality of semiconductor regions of said first conductivity type and said plurality of semiconductor regions of said second conductivity type, and wherein at the conclusion of said step of filling the bottom portion of said grooves, said gate laterally surrounds said plurality of semiconductor regions of said first and second conductivity type.

REMARKS

Applicant has added Claim 18 directed towards a method for manufacturing a transistor in which a groove laterally surrounds the plurality of regions of a first and second con-